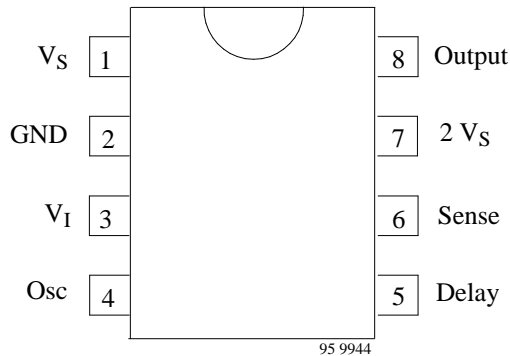




## Pin Description



Pin	Symbol	Function
1	$V_S$	Supply voltage $V_S$
2	GND	IC ground
3	$V_I$	Control input (duty cycle)
4	Osc	Oscillator
5	Delay	Short circuit protection delay
6	Sense	Current sensing
7	$2 V_S$	Voltage doubler
8	Output	Output

## Functional Description

### Supply Voltage, $V_S$ or $V_{Batt}$ , Pin 1

### GND Pin 2

### Control Input, Pin 3

The pulse width is controlled by means of an external potentiometer (47 k $\Omega$ ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 0 to 100%. To avoid inadmissibly high filament cold currents, the dimmer is switched off at duty cycles of approximately < 10% or is switched on only at duty cycles of approximately > 13% (hysteresis). It is possible to further restrict the duty cycle with the resistors  $R_1$  and  $R_2$ . Pin 3 is protected against short-circuit to  $V_{Batt}$  and ground GND ( $V_{Batt} \leq 16.5$  V).

### Output Slope Control

The rise and fall time ( $t_r$ ,  $t_f$ ) of the lamp voltage can be limited to reduce radio interference. This is done with an integrator which controls a power MOSFET as source follower. The slope time is controlled by an external capacitor and the oscillator current.

Calculation:

$$t_r = t_f = V_{Batt} \cdot \frac{C_4}{I_{osc}}$$

With  $V_{Batt} = 12$  V,  $C_4 = 470$  pF and  $I_{osc} = 40$   $\mu$ A, we thus obtain a controlled slope of

$$t_r = t_f = 12 \text{ V} \cdot \frac{470 \text{ pF}}{40 \text{ } \mu\text{A}} = 141 \text{ } \mu\text{s}$$

### Oscillator, Pin 4

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor,  $C_2$ . It is

charged with a constant current,  $I$ , until the upper switching threshold is reached. A second current source is then activated which taps a double current,  $2 I$ , from the charging current. The capacitor,  $C_2$ , is thus discharged by the current,  $I$ , until the lower switching threshold is reached. The second source is then switched off again and the procedure starts again.

### Example for oscillator frequency calculation:

$$V_{T100} = V_S \cdot \alpha_1 = (V_{Batt} - I_S \cdot R_3) \cdot \alpha_1$$

$$V_{T<100} = V_S \cdot \alpha_2 = (V_{Batt} - I_S \cdot R_3) \cdot \alpha_2$$

$$V_{TL} = V_S \cdot \alpha_3 = (V_{Batt} - I_S \cdot R_3) \cdot \alpha_3$$

where

$$V_{T100} = \text{High switching threshold (100% duty cycle)}$$

$$V_{T<100} = \text{High switching threshold (< 100% duty cycle)}$$

$$V_{TL} = \text{Low switching threshold}$$

$\alpha_1$ ,  $\alpha_2$  and  $\alpha_3$  are fixed constant.

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

$$V_{Batt} = 12 \text{ V}, I_S = 4 \text{ mA}, R_3 = 150 \text{ } \Omega, \\ \alpha_1 = 0.7, \alpha_2 = 0.67 \text{ and } \alpha_3 = 0.28.$$

$$V_{T100} = (12 \text{ V} - 4\text{mA} \cdot 150\Omega) \cdot 0.7 \approx 8 \text{ V}$$

$$V_{T<100} = 11.4 \text{ V} \cdot 0.67 = 7.6 \text{ V}$$

$$V_{TL} = 11.4 \text{ V} \cdot 0.28 = 3.2 \text{ V}$$

For a duty cycle of 100%, an oscillator frequency,  $f$ , is as follows:

$$f = \frac{I_{osc}}{2 \cdot (V_{T100} - V_{TL}) \cdot C_2}, \text{ whereas } C_2 = 22 \text{ nF} \\ \text{and } I_{osc} = 40 \text{ } \mu\text{A}$$

Therefore:

$$f = \frac{40 \text{ } \mu\text{A}}{2 \cdot (8 \text{ V} - 3.2 \text{ V}) \cdot 22 \text{ nF}} = 189 \text{ Hz}$$

For a duty cycle of less than 100%, the oscillator frequency,  $f$ , is as follows:

$$f = \frac{I_{osc}}{2 \cdot (V_{T<100} - V_{TL}) \cdot C_2 + 2 \cdot V_{Batt} \cdot C_4} \\ \text{whereas } C_4 = 470 \text{ pF} \\ = \frac{I_{osc}}{2 \cdot (7.6 \text{ V} - 3.2 \text{ V}) \cdot 22 \text{ nF} + 2 \cdot 12 \text{ V} \cdot 470 \text{ pF}} \\ = 195 \text{ Hz}$$

A selection of different values of  $C_2$  and  $C_4$ , provides a range of oscillator frequency,  $f$ , from 10 to 2000 Hz.

## Short-Circuit Protection and Current Sensing, Pins 5 and 6

### 1. Short-Circuit Detection and Time Delay, $t_d$

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ( $V_{T2} \approx 90 \text{ mV}$ ), the duty cycle is switched over to 100% and the capacitor  $C_5$  is charged by a current source of  $20 \text{ } \mu\text{A}$  ( $I_{dis} - I_{ch}$ ). The external FET is switched off after the cut-off threshold ( $V_{TL}$ ) is reached. Renewed switching on the FET is

possible only after a power-on reset. The current source,  $I_{ch}$ , ensures that the capacitor  $C_5$  is not charged by parasitic currents. The capacitor  $C_5$  is discharged by  $I_{ch}$  to typ.  $0.7 \text{ V}$ .

Time delay,  $t_d$ , is as follows:

$$t_d = C_5 \cdot (V_{TL} - 0.7 \text{ V}) / (I_{dis} - I_{ch})$$

With  $C_5 = 330 \text{ nF}$  and  $V_{TL} = 9.8 \text{ V}$ , ( $I_{dis} - I_{ch}$ ) =  $20 \text{ } \mu\text{A}$ , we have

$$t_d = 330 \text{ nF} \cdot (9.8 \text{ V} - 0.7 \text{ V}) / 20 \text{ } \mu\text{A} \\ = 150 \text{ ms.}$$

## Charge Pump and Output, Pins 7 and 8

Output, Pin 8, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor  $C_3$  (bootstrapping). Additionally, a trickle charge is generated by an integrated oscillator ( $f_7 \approx 400 \text{ kHz}$ ) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

## Undervoltage Detection

In the event of voltages of approximately  $V_{Batt} < 5.0 \text{ V}$ , the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately  $V_{Batt} \geq 5.4 \text{ V}$ .

## Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a  $820 \text{ k}\Omega$  resistor between gate and source it is recommended to provide proper switch-off conditions.

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	$V_S$	25	V
Junction temperature	$T_j$	150	°C
Ambient temperature range	$T_{amb}$	-40 to +110	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C

## Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient	$R_{thJA}$	120	K/W

## Electrical Characteristics

$T_{amb} = -40$  to  $+110^{\circ}\text{C}$ ,  $V_{Batt} = 9$  to  $16.5$  V, (Basic function is guaranteed between  $6.0$  V to  $9.0$  V) reference point GND, unless otherwise specified (see figure 1).

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Current consumption	Pin 1	$I_S$			6.8	mA
Supply voltage	Overvoltage detection, stage 1	$V_{Batt}$			25	V
Stabilized voltage	$I_S = 10$ mA Pin 1	$V_Z$	24.5		27.0	V
Battery undervoltage detection	ON OFF	$V_{Batt}$	4.4 4.8	5.0 5.4	5.6 6.0	V
<b>Oscillator</b> $f = 10$ to $2000$ Hz Pin 4						
Threshold cycle Upper  Lower	$V_8 = \text{High}, \alpha_1 = \frac{V_{T100}}{V_S}$	$\alpha_1$	0.68	0.7	0.72	
	$V_8 = \text{Low}, \alpha_2 = \frac{V_{T<100}}{V_S}$	$\alpha_2$	0.65	0.67	0.69	
	$\alpha_3 = \frac{V_{TL}}{V_S}$	$\alpha_3$	0.26	0.28	0.3	
Constant oscillator current	$V_{Batt} = 12$ V	$\pm I_{Osc}$	26	40	54	$\mu\text{A}$
Frequency tolerance	$C_4$ open, $C_2 = 470$ nF, duty cycle = 50%	$\Delta f$	6.0	9.9	13.5	Hz
Stabilized voltage	$I_S = 30$ mA Pin 1	$V_Z$	18.5	20.0	21.5	V
<b>Gate output</b> Pin 8						
Voltage	Low level	$V_8$	0.35	0.70	0.95	V
	$V_{Batt} = 16.5$ V, $T_{amb} = 110^{\circ}\text{C}$ , $R_3 = 150$ $\Omega$				1.5	
	High level, duty cycle 100%	$V_8$		$V_7$		
Current	$V_8 = \text{Low level}$	$I_8$	1.0			mA
	$V_8 = \text{High level}, I_7 >  I_8 $		-1.0			
<b>Short-circuit protection</b> Pin 6						
Short-circuit current regulation	$V_{T1} = V_S - V_6$	$V_{T1}$	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$	$V_{T2}$	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	mV
<b>Short circuit recognition,</b> $V_{Batt} = 12$ V Pin 5						
Switched off threshold	$V_{TL} = V_S - V_5$	$V_{TL}$	9.5	9.8	10.1	V
Charge current		$I_{ch}$		23		$\mu\text{A}$
Dicharge current		$I_{dis}$		3		$\mu\text{A}$
Capacitance current	$I_5 = I_{ch} - I_{dis}$	$I_5$	13	20	27	mA
<b>Voltage doubler</b> Pin 7						
Voltage	Duty cycle 100%	$V_7$	$2 V_S$			
Oscillator frequency		$f_7$	280	400	520	kHz
Internal voltage limitation	$I_7 = 5$ mA	$V_7$	26	27.5	30.0	V
	or whichever is lower	$V_7$	$V_{S+14}$	$V_{S+15}$	$V_{S+16}$	
<b>Switch-off at small duty cycles</b> $V_{Batt} = 12$ V Pin 3						
Output disabled		$V_3/V_S$	0.3	0.32	0.34	
Output active		$V_3/V_S$	0.32	0.34	0.36	
Hysteresis switch-on		$\Delta V_3/V_S$	0.004		0.032	

## Application

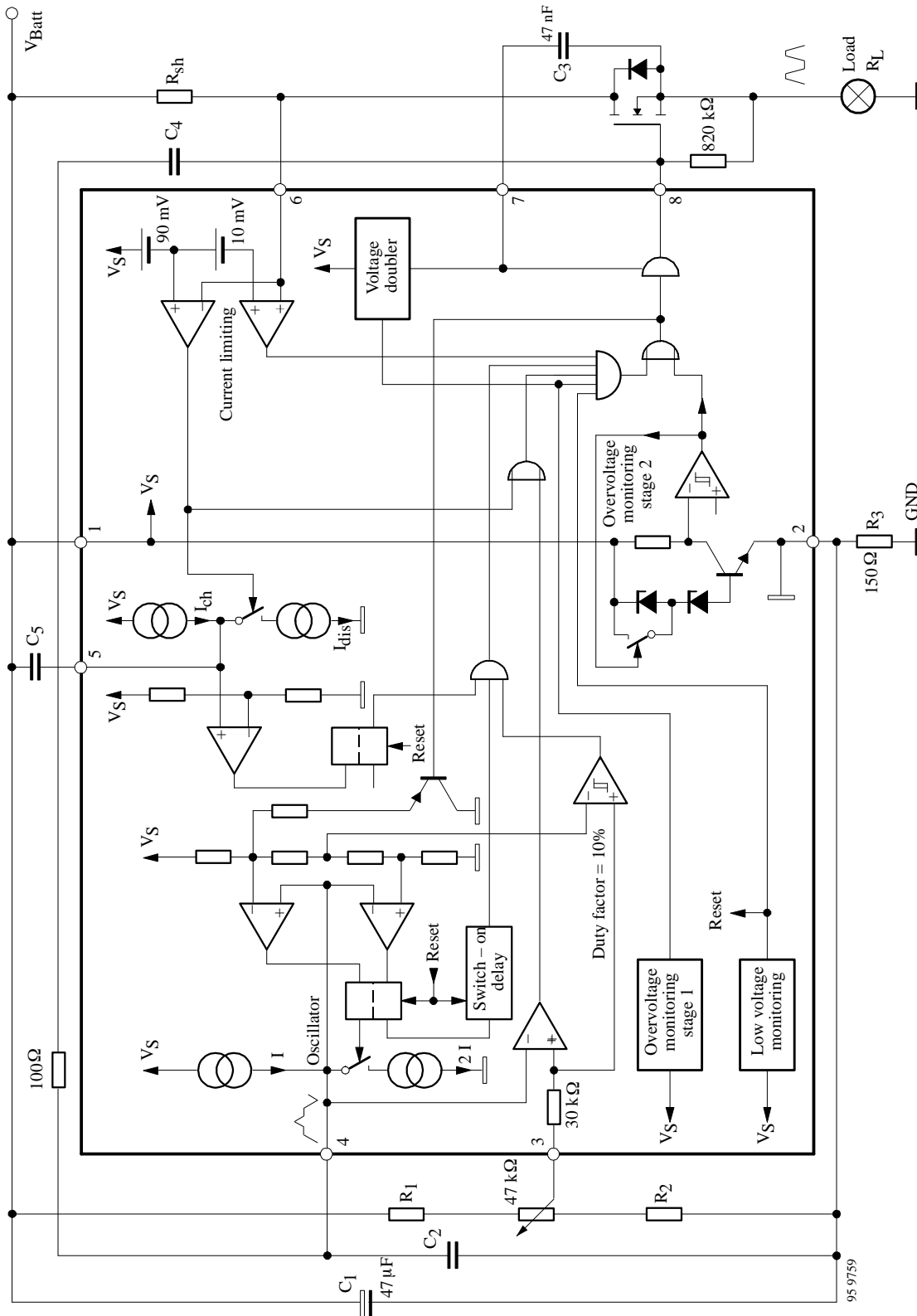


Figure 2.

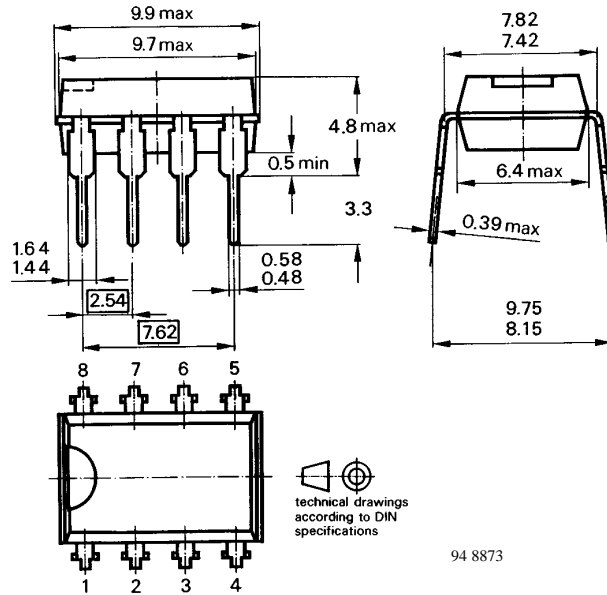
# U6081B

# TEMIC

TELEFUNKEN Semiconductors

## Dimensions in mm

Package: DIP 8



## Ozone Depleting Substances Policy Statement

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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**TEMIC TELEFUNKEN microelectronic GmbH** semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**TEMIC** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design without further notice.**

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